REDUCED POWER REDUNDANCY ADDRESS DECODER AND COMPARISON CIRCUIT

ABSTRACT OF THE DISCLOSURE

A redundancy address decoder for a memory having at least one bank of memory segmented into a plurality of memory blocks. The redundancy address decoder includes a plurality of redundancy comparison circuitry coupled to a respective programmable element block storing addresses that are mapped to redundant memory of a memory plane. The redundancy address decoder further includes redundancy driver select logic coupled to each of the redundancy comparison circuitry to activate a selected one of the redundancy comparison circuitry for comparing a portion of a memory address corresponding to a memory location with the programmed addresses of the respective programmable element blocks, which leads to power reduction for column accesses to the memory device. The selection of the redundancy driver is based on the memory bank in which the memory location is located.